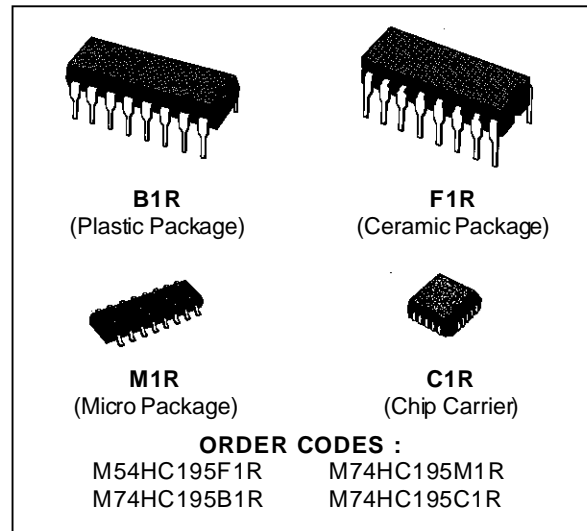


8 BIT PIPO SHIFT REGISTER

- HIGH SPEED
 $t_{PD} = 13 \text{ ns (TYP.) at } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25 \text{ }^\circ\text{C } 6 \text{ V}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ V to } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS195



DESCRIPTION

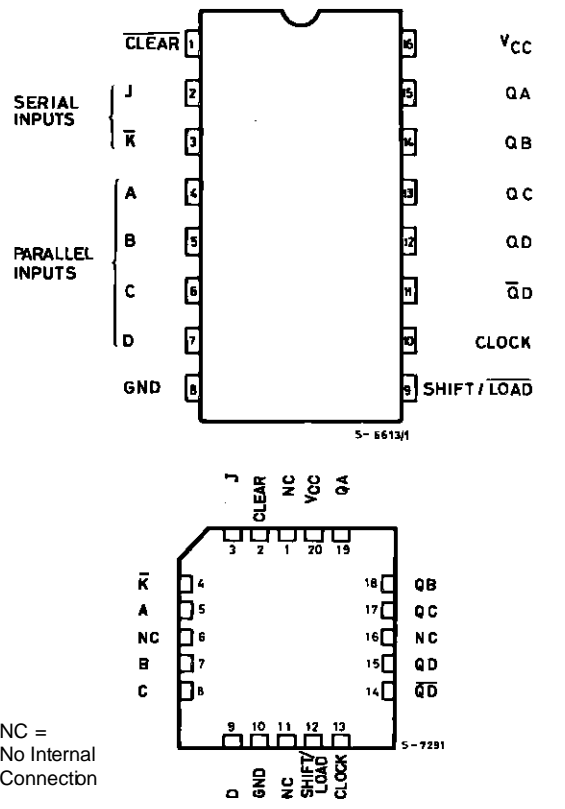
The M54/74HC195 is a high speed CMOS 4 BIT PIPO SHIFT REGISTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This shift register features parallel inputs, parallel outputs, J-K serial inputs, a SHIFT/LOAD control input, and a direct overriding CLEAR. This shift register can operate in two modes : Parallel Load ; Shift from QA towards QD.

Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/LOAD control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/LOAD control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K or TOGGLE flip flop as shown in the truth-table.

All inputs are equipped with protection circuits against static discharge transient excess voltage.

PIN CONNECTIONS (top view)



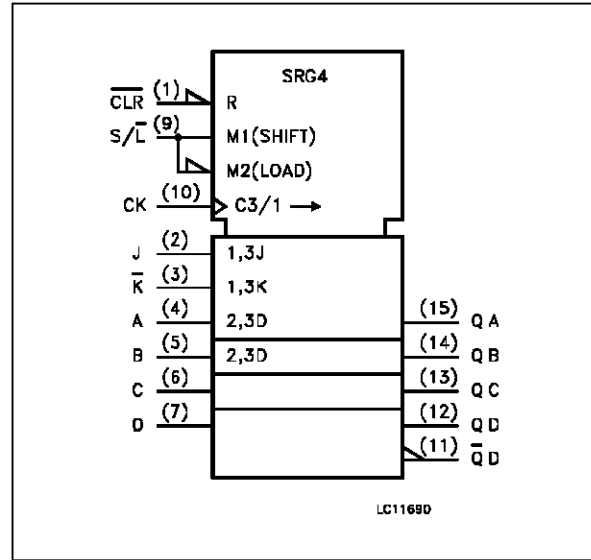
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Reset Input (Active LOW)
2	J	First Stage J Input (Active LOW)
3	$\overline{\text{K}}$	First Stage $\overline{\text{K}}$ Input (Active LOW)
4, 5, 6, 7	A to D	Parallel Data Input
9	SHIFT/ $\overline{\text{LOAD}}$	Control Input
10	CLOCK	Clock Input (LOW to HIGH Edge-triggered)
11	$\overline{\text{QD}}$	Inverted Output From The Last Stage
15, 14, 13, 12	QA to QD	Paralle Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOL

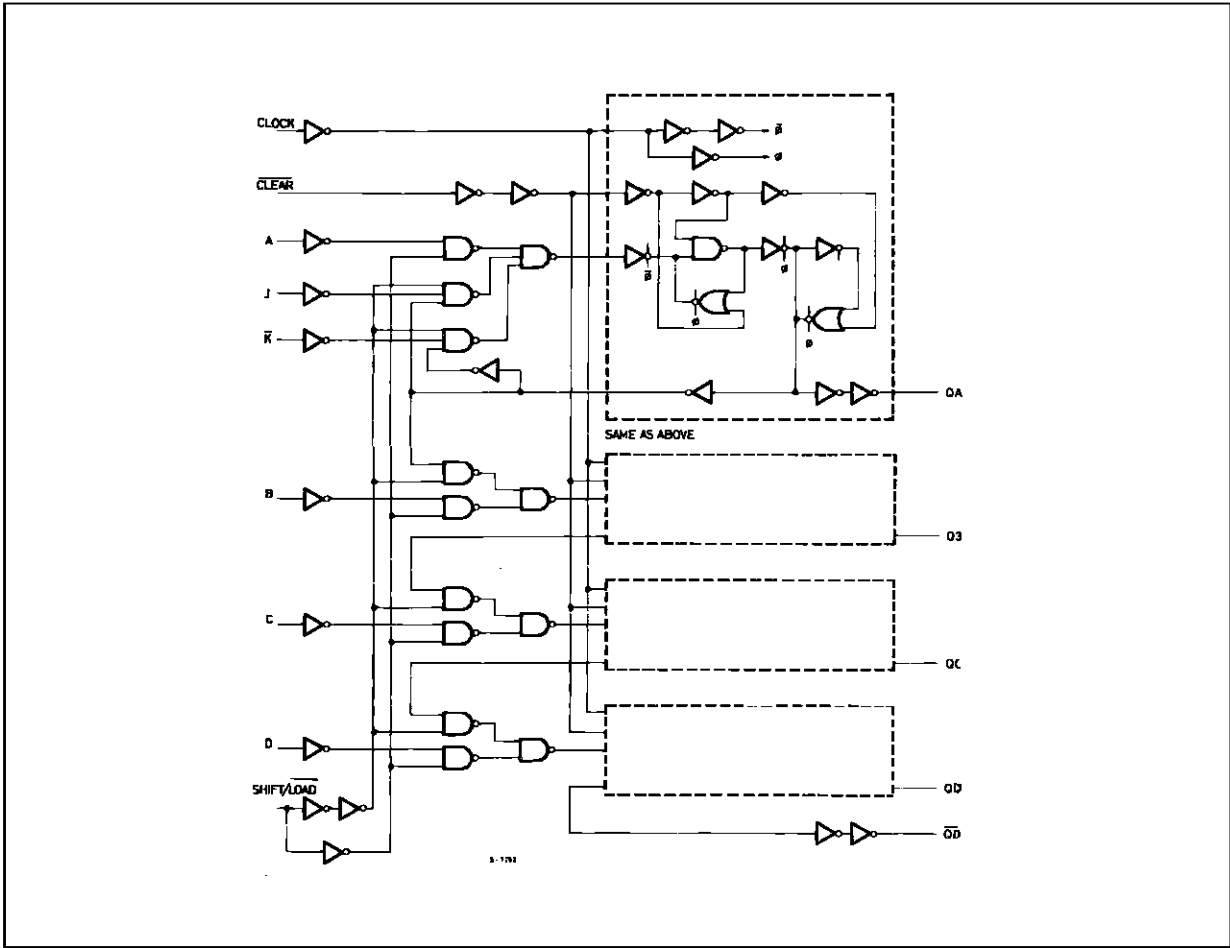


TRUTH TABLE

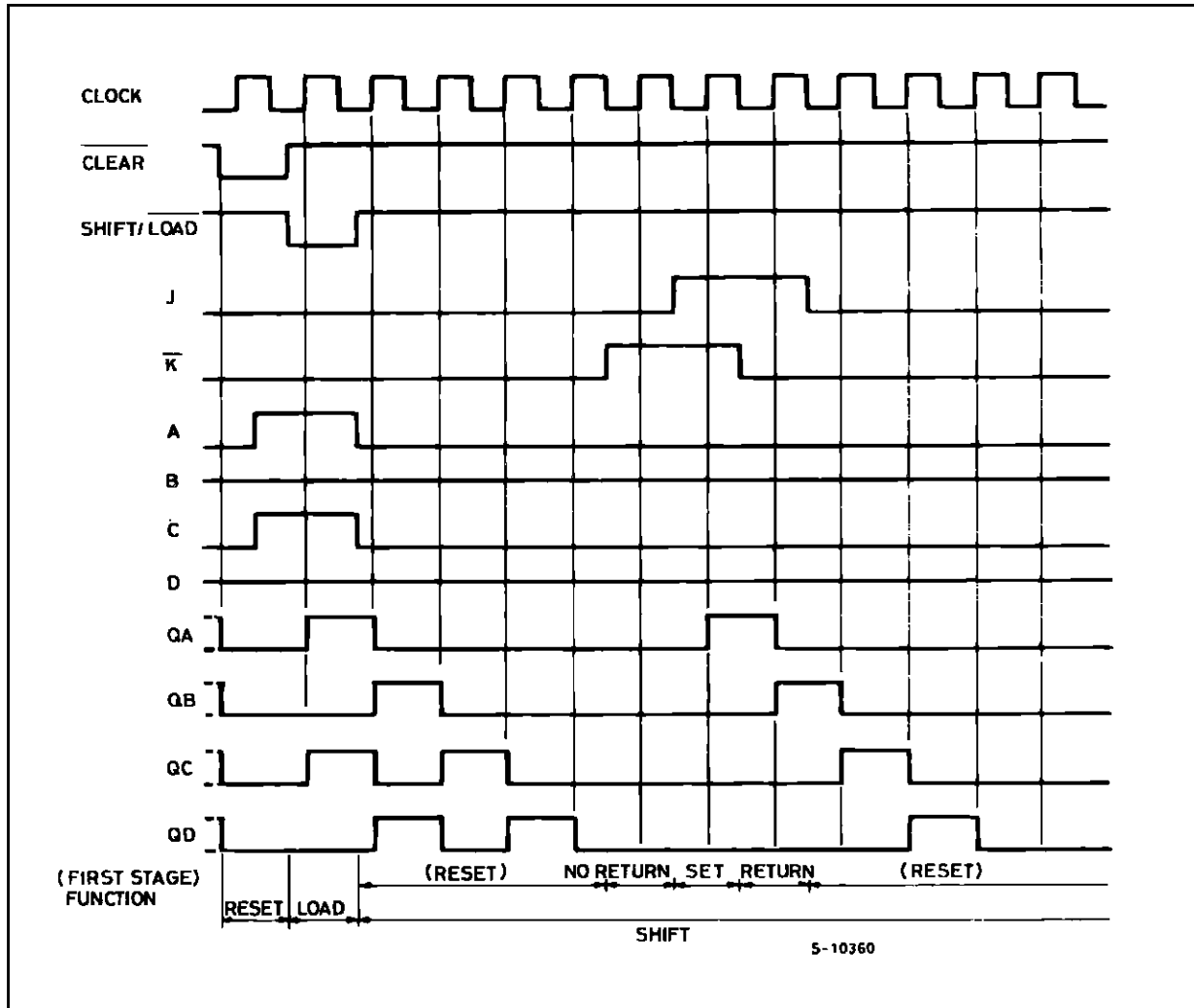
CLEAR	SHIFT/LOAD	CLOCK	INPUTS						OUTPUTS				
			SERIAL		PARALLEL				QA	QB	QC	QD	$\overline{\text{QD}}$
			J	$\overline{\text{K}}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L		X	X	a	b	c	d	a	b	c	d	\overline{d}
H	H	$\overline{\text{L}}$	X	X	X	X	X	X	QA0	QB0	QC0	QD0	$\overline{\text{QD0}}$
H	H		L	H	X	X	X	X	QA0	QA0	QBn	QCn	$\overline{\text{QCn}}$
H	H		L	L	X	X	X	X	L	QAn	QBn	QCn	$\overline{\text{QCn}}$
H	H		H	H	X	X	X	X	H	QAn	QBn	QCn	$\overline{\text{QCn}}$
H	H		H	L	X	X	X	X	$\overline{\text{QAn}}$	QAn	QBn	QCn	$\overline{\text{QCn}}$

X: Don't Care: The level of QA, QB, QC, respectively, before the most recent positive transition of the clock.

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	2 to 6	V	
V _I	Input Voltage	0 to V _{CC}	V	
V _O	Output Voltage	0 to V _{CC}	V	
T _{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C	
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2 V V _{CC} = 4.5 V V _{CC} = 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

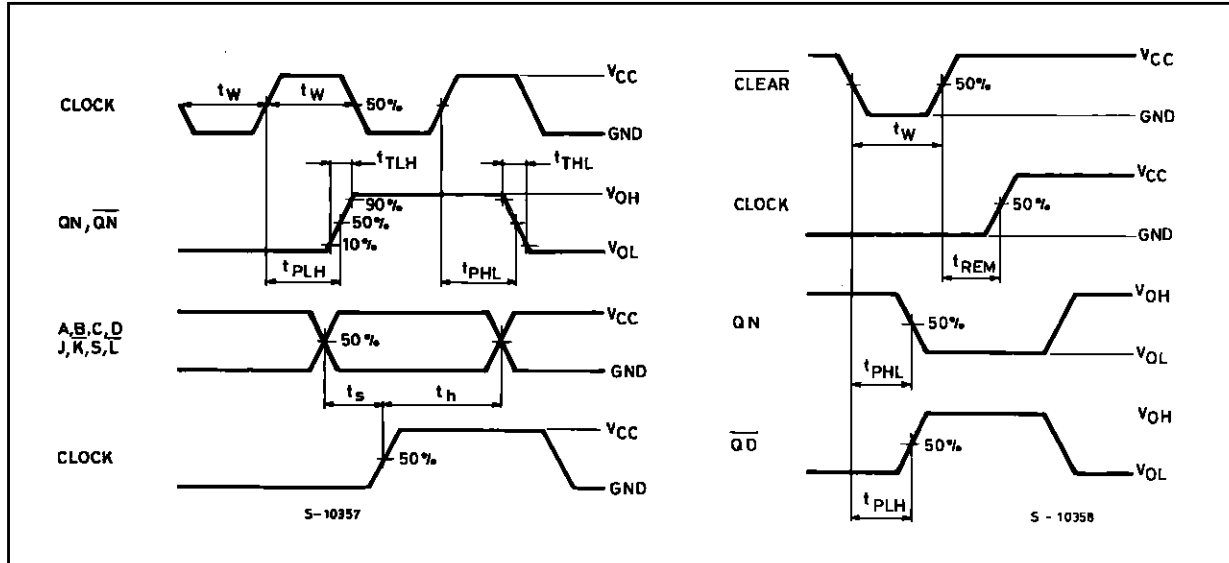
Symbol	Parameter	Test Conditions		Value						Unit		
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5	I _O = -4.0 mA	4.18	4.31		4.13		4.10			
		6.0		I _O = -5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I _O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0			I _O = 5.2 mA		0.18	0.26		0.33		
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

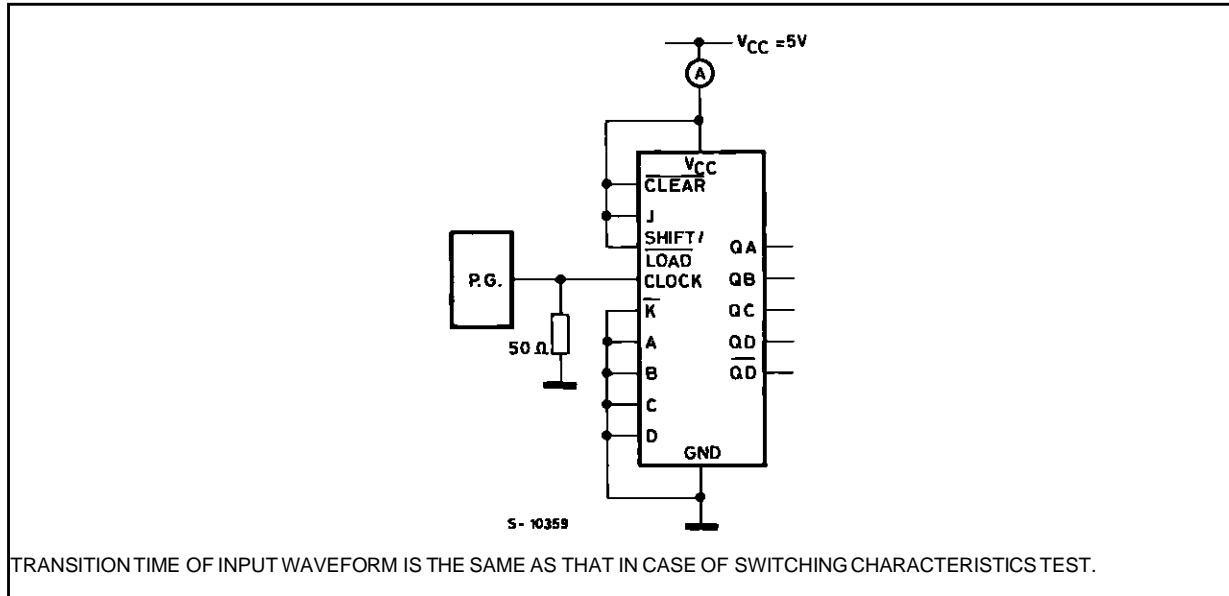
Symbol	Parameter	Test Conditions		Value						Unit	
		V_{CC} (V)		$T_A = 25\text{ }^\circ\text{C}$ 54HC and 74HC			-40 to $85\text{ }^\circ\text{C}$ 74HC		-55 to $125\text{ }^\circ\text{C}$ 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK- Q_n , \overline{QD})	2.0			48	125		155		190	ns
		4.5			16	25		31		38	
		6.0			14	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR- Q_n , \overline{QD})	2.0			45	120		150		180	ns
		4.5			15	24		30		36	
		6.0			13	20		26		31	
f_{MAX}	Maximum Clock Frequency	2.0		7.6	15		6		5		MHz
		4.5		38	60		30		25		
		6.0		45	71		35		30		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			20	75		95		115	ns
		4.5			5	15		19		23	
		6.0			4	13		16		20	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0			20	75		95		115	ns
		4.5			5	15		19		23	
		6.0			4	13		16		20	
t_s	Minimum Set-up Time (PI)	2.0			28	75		95		115	ns
		4.5			7	15		19		23	
		6.0			6	13		16		20	
t_s	Minimum Set-up Time (J, K, S/L)	2.0			28	75		95		115	ns
		4.5			7	15		19		23	
		6.0			6	13		16		20	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				72						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

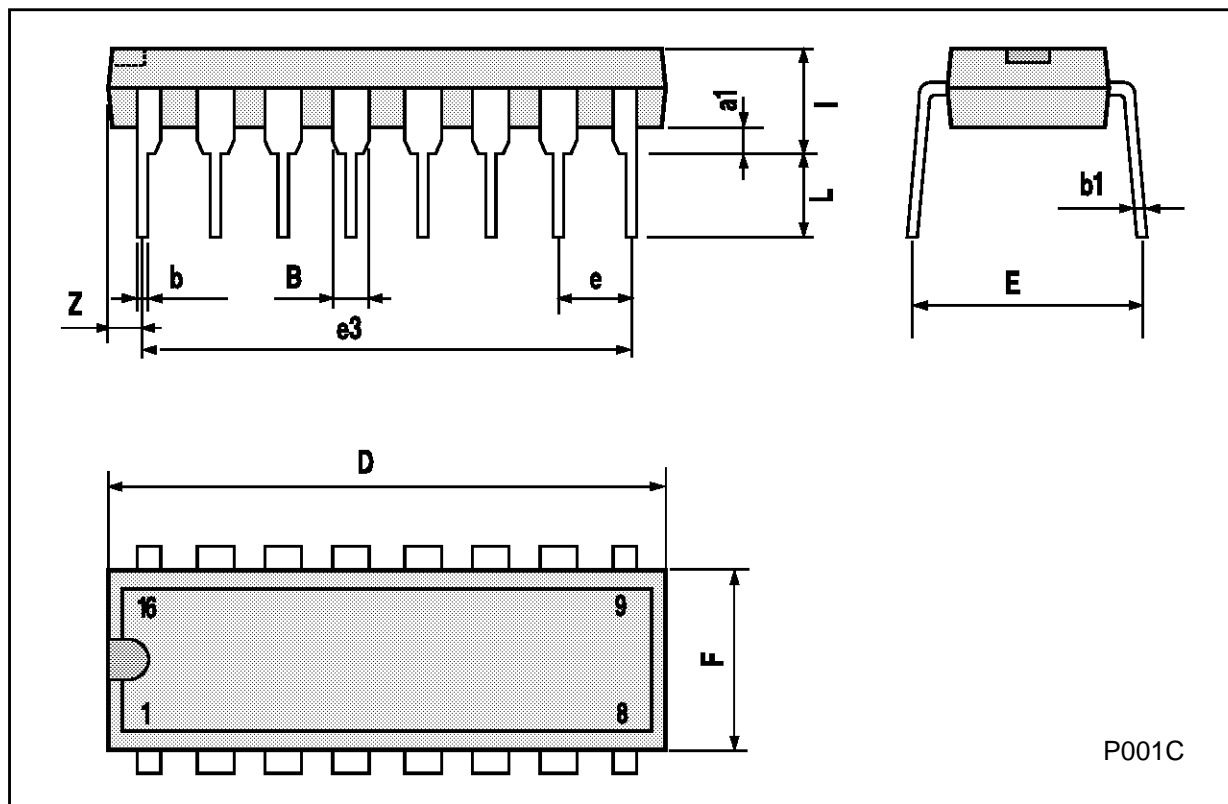


TEST CIRCUIT I_{CC} (Opr.)



Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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